R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR AMENDMENTS TO THE CLAIMS

Support for new claims 21-23 can be found in the drawings as originally filed. for example, on FIGS. 1 and 2, and in the specification, page 3, line 17, through page 6, line 2. Support for new claims 24-29 can be found in the drawings as originally filed, for example, on FIGS. 3 and 4, and in the specification, page 6, lines 3, through page 12). As such no new matter was added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 4 and 6-20 under 35 U.S.C. §102 as being anticipated by Agrawal '884 has been obviated by appropriate amendment and should be withdrawn.

Agrawal discloses a multiple array high performance programmable logic device family (Title).

In contrast, claim 21 of the present invention provides an apparatus comprising a first programmable interconnect matrix and a second programmable interconnect matrix. The first programmable interconnect matrix includes one or more first multiplexers that may be configured to (i) receive a distributed

input group of signals in a first order and (ii) present the distributed input group of signals in a second order. The second programmable interconnect matrix includes one or more second multiplexers that may be configured to receive the distributed input group of signals from the first programmable interconnect matrix in the second order. The first order of signals are different from the second order of said signals. The second order of signals are disposed in an input-re-order channel.

Claim 24 of the present invention provides an apparatus comprising a first distributed multiplexer and a second distributed multiplexer. The first distributed multiplexer may be configured to generate a first output in response to (i) a first portion coupled to a first group of input signals and (ii) a second portion coupled to a second group of input signals. The second distributed multiplexer may be configured to generate a second output in response to a (i) a first portion coupled to a third group of input signals and (ii) a second portion coupled to a fourth group of input signals. The first portion of the first distributed multiplexer may be physically separated from the second portion of the first distributed multiplexer on a layout area. The first portion of the second distributed multiplexer may be physically separated from the second portion of the second distributed multiplexer on the layout area.

With respect to claim 21, Agrawal fails to disclose the presently claimed first programmable interconnect matrix having one or more first multiplexers configured to (i) receive a distributed input group of signals in a first order and present the distributed input group of signals in a second order. Agrawal merely discloses a group of inputs and outputs presented to a macrocell 43, 60 and 61 in the Quadrant B in a first order, and the macrocells 43, 60 and 61 being presented to the local buses 44B, 44C and to the macrocells 43, 60 and 61 (see Agrawal, FIGS. 2A' and 2A'') in the same first order. Agrawal is silent on the presently claimed one or more first multiplexers configured to receive a distributed input group of signals in a first order and present the distributed input group of signals in a second order. Therefore, the presently claimed invention is fully patentable over Agrawal and the rejection should be withdrawn.

Moreover, Agrawal fails to disclose the presently claimed second programmable interconnect matrix having one or more second multiplexers configured to receive the distributed input group of signals from the first programmable interconnect matrix in the second order. Finally, Agrawal fails to disclose the second order of the distributed input group of signals being disposed in an input-re-order channel. Therefore, the presently claimed invention is fully patentable over Agrawal and the rejection should be withdrawn.

With respect to claim 24, Agrawal fails to disclose the presently claimed first distributed multiplexer configured to generate a first output in response to a first portion and a second portion where the first portion of first distributed multiplexer is physically separated from the second portion of the first distributed multiplexer on a layout area. In particular, Agrawal is silent on physically separating portions of a multiplexer to form distributive multiplexers on a layout area. Therefore, the presently claimed invention is fully patentable over Agrawal and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 2, 3 and 5 under 35 U.S.C. §103 as being unpatentable over Agrawal in view of Graf is respectfully obviated by appropriate amendment and should be withdrawn. Claims 2 and 5 depend, directly or indirectly from new claim 21, which is now believed to be allowable. Claim 3 has been canceled.

As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Christopher P. Maiorana
Registration No. 42,829
24840 Harper Avenue, Suite 100
St. Clair Shores, MI 48080
(586) 498-0670

Dated: August 16, 2005

Docket No.: 0325.00504